

IN THE CLAIMS

Please cancel claims 16-18 and 22-23.

Please amend the claims as follows.

- 1 1. (Original) An apparatus comprising:
2 at least one processor;
3 a memory coupled to the at least one processor;
4 an integrated circuit design residing in the memory, the integrated circuit design
5 including a plurality of logic blocks;
6 a static timing tool residing in the memory and executed by the at least one
7 processor, the static timing tool performing analysis that results in a plurality of slack
8 computations;
9 a timing analysis mechanism residing in the memory and executed by the at least
10 one processor, the timing analysis mechanism including a dummy edge mechanism that
11 creates a dummy clock test edge for a selected logic block that has a clock test signal and
12 a data launch signal that are on opposite edges in a manner that results in the dummy
13 clock test edge and the data launch signal being on the same edge, the static timing tool
14 automatically identifying in the integrated circuit design at least one common logic block
15 through which the clock test signal and the data launch signal both pass before arriving at
16 the selected logic block, the timing analysis mechanism automatically improving at least
17 one of the plurality of slack computations due to the at least one common logic block.
- 1 2. (Original) The apparatus of claim 1 wherein the static timing tool is EinsTimer.
- 1 3. (Original) The apparatus of claim 1 wherein the timing analysis mechanism
2 determines a difference between fastest and slowest delay through the at least one
3 common logic block, multiplies the difference by a correction factor, and adjusts the slack
4 by the difference multiplied by the correction factor.

1 4. (Original) The apparatus of claim 1 wherein the timing analysis mechanism improves
2 at least one of the plurality of slack computations using at least one user delta adjust
3 parameter to adjust the clock test signal.

1 5. (Original) The apparatus of claim 1 wherein the timing analysis mechanism provides
2 input to the static timing tool but is not part of the static timing tool.

1 6. (Original) An apparatus comprising:
2 at least one processor;
3 a memory coupled to the at least one processor;
4 an integrated circuit design residing in the memory, the integrated circuit design
5 including a plurality of logic blocks;
6 a static timing tool residing in the memory and executed by the at least one
7 processor, the static timing tool performing analysis that results in a plurality of slack
8 computations; and
9 a timing analysis mechanism residing in the memory and executed by the at least
10 one processor, the timing analysis mechanism being separate from the static timing tool
11 and providing input to the static timing tool, wherein the timing analysis mechanism
12 creates a dummy clock test edge for a selected logic block that has a clock test signal and
13 a data launch signal that are on opposite edges in a manner that results in the dummy
14 clock test edge and the data launch signal being on the same edge, the static timing tool
15 automatically identifying in the integrated circuit design at least one common logic block
16 through which the clock test signal and the data launch signal both pass before arriving at
17 the selected logic block, the timing analysis mechanism automatically improving at least
18 one of the plurality of slack computations due to the at least one common logic block
19 using at least one user delta adjust parameter to adjust the clock test signal.

1 7. (Original) The apparatus of claim 6 wherein the static timing tool is EinsTimer.

1 8. (Original) The apparatus of claim 6 wherein the timing analysis mechanism
2 determines a difference between fastest and slowest delay through the at least one
3 common logic block, multiplies the difference by a correction factor, and adjusts the slack
4 by the difference multiplied by the correction factor.

1 9-14 (Cancelled)

1 15. (Currently Amended) A computer readable program product comprising:
2 a timing analysis mechanism that includes a dummy edge mechanism that creates
3 a dummy clock test edge for a selected logic block in an integrated circuit design, the
4 selected logic block having a clock test signal and a data launch signal that are on
5 opposite edges, the dummy edge mechanism creating the dummy clock test edge so the
6 dummy clock test edge and the data launch signal are on the same edge, the timing
7 analysis mechanism automatically identifying in the integrated circuit design at least one
8 common logic block through which the clock test signal and the data launch signal both
9 pass before arriving at the selected logic block, the timing analysis mechanism
10 automatically improving at least one of [[the]] a plurality of slack computations due to the
11 at least one common logic block; and
12 ~~computer readable signal bearing~~ recordable media bearing the timing analysis
13 mechanism.

1 16-18 (Cancelled)

1 19. (Currently Amended) The program product of claim 15 wherein the timing analysis
2 mechanism determines a difference between fastest and slowest delay through the at least
3 one common logic block, multiplies the difference by a correction factor, and adjusts the
4 at least one slack computation by the difference multiplied by the correction factor.

1 20. (Original) The program product of claim 15 wherein the timing analysis mechanism
2 improves at least one of the plurality of slack computations using at least one user delta
3 adjust parameter to adjust the clock test signal.

1 21. (Currently Amended) A computer readable program product comprising:
2 a timing analysis mechanism that is separate from a static timing tool and that
3 provides input to the static timing tool, the timing analysis mechanism creating a dummy
4 clock test edge for a selected logic block that has a clock test signal and a data launch
5 signal that are on opposite edges in a manner that results in the dummy clock test edge
6 and a data launch signal on a logic block in an integrated circuit design occurring on the
7 same edge, the timing analysis mechanism automatically identifying in the integrated
8 circuit design at least one common logic block through which the clock test signal and the
9 data launch signal both pass before arriving at the selected logic block, the timing
10 analysis mechanism automatically improving at least one of [[the]] a plurality of slack
11 computations due to the at least one common logic block using at least one user delta
12 adjust parameter to adjust the clock test signal; and
13 ~~computer readable signal bearing~~ recordable media bearing the timing analysis
14 mechanism.

1 22-23 (Cancelled)

1 24. (Original) The program product of claim 21 wherein the static timing tool is
2 EinsTimer.

1 25. (Currently Amended) The program product of claim 21 wherein the timing analysis
2 mechanism determines a difference between fastest and slowest delay through the at least
3 one common logic block, multiplies the difference by a correction factor, and adjusts the
4 at least one slack computation by the difference multiplied by the correction factor.

STATUS OF THE CLAIMS

Claims 1-25 were originally filed in this patent application. An office action dated 07/03/2006 included a restriction requirement. In response, an Election of Claims and Amendment was filed on 08/02/2006 that elected claims 1-8 and 15-25, and cancelled claims 9-14. In the pending office action, claims 15 and 21 were rejected under 35 U.S.C. §101, claims 15-25 were rejected under 35 U.S.C. §112, second paragraph, and claims 1-8 and 15-25 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting. No claim was allowed. In this amendment, claims 16-18 and 22-23 have been cancelled, and claims 15, 19, 21 and 25 have been amended. Claims 1-8, 15, 19-21 and 24-25 are currently pending.